Digital Control Strategy for Multi-Phase Interleaved Boundary Mode and DCM Boost PFC Converters

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Abstract— A digital control strategy which provides optimal interleaving of multi-phase boost power factor correction (PFC) rectifiers operating at DCM/CCM boundary (BCM) or in DCM is presented in this paper. In this method two feedforward algorithms are used. The first provides the turn-on time to attain the desired input current and the second computes the switching period time to achieve BCM operation. An extension to operate in DCM is proposed to avoid CCM under all conditions. Regulated DCM is used to realize a new continuous phase shedding method, which is used to limit the switching frequency. The proposed control structure was implemented on a microcontroller. Experimental results show the effectiveness of the control strategy on a boost PFC prototype with 3 parallel rails.

Index Terms— Continuous phase shedding, boundary conduction mode (BCM), discontinuous conduction mode, feedforward control, interleaving, power factor correction (PFC).

I. INTRODUCTION

For high efficiency the boost power factor correction (PFC) rectifiers operating in discontinuous conduction mode (DCM) or boundary conduction mode (BCM) is the preferred topology [1-3]. Compared to the continuous conduction mode (CCM) the reverse-recovery losses of the boost diode are eliminated. Thus, low cost Si-diodes can be used. Due to turn-on of the boost switch with zero-voltage switching (ZVS) or near ZVS also the switching losses can be reduced.

However, the power level of PFC converters operated in DCM or BCM is limited up to 300-400W [2]. While BCM operation implies variable switching frequency, DCM boost PFC converter can be operated with constant as well as with variable switching frequency. Compared to DCM with constant switching frequency, BCM yields in lower total harmonic distortion (THD) of the input current and smaller peak inductor currents resulting in lower switching and conduction losses [1]. In a digital control structure BCM and DCM with variable switching frequency can be achieved with predictive control algorithms [4, 5].

To attain higher power levels two or more converters should be operated interleaved. In addition interleaving provides good current ripple cancelation, resulting in smaller and cheaper EMI filters. However, synchronized interleaved BCM with variable switching frequency is challenging and topic of several publications, e.g. [1-3, 6]. Most of the published interleaving strategies focus on only two paralleled converters, for which reason the power level is still limited up to 600-800W.

Relatively complex analog circuitry is required to implement those concepts. Mostly, constant on-time is used to achieve sinusoidal current shape and the zero-crossing detection of every inductor current is required to turn on the
The phase shift of 180° is realized by considering the previous switching periods.

In this paper a digital control strategy is presented which enables interleaving of multi-phase PFC converters (cf. Fig. 1). Feedforward control algorithms are used to achieve BCM or DCM operation by computing the switch-on-time and the switching period. Depending on the inductance and the input voltage the on-time is computed to attain the desired input current. Using the on-time, the input and output voltage the required period time is calculated to ensure BCM or rather DCM operation. From the switching period the required phase shift value is determined to guarantee optimal ripple cancelation. The current tracking via the on-time calculation can be done by a feedforward open-loop algorithm or with an additional closed-loop current controller. With open-loop control no current sensing is necessary while with closed-loop control it suffices to measure only the overall input current with a common shunt sensor.

Due to the fact that the inductor current returns to zero in the off-time, the inductance value is essential for BCM operation. Due to the fact that the inductor current returns to zero in the off-time, an exact knowledge of this value is not necessary while with closed-loop control it suffices to measure only the overall input current with a common shunt sensor.

At light load phase shedding is applied to increase the efficiency by decreasing the number of energized converters. Due to the fact that the inductor current returns to zero in every switching cycle, phase shedding can be applied at any time. This enables the possibility to change the number of energized phases not only depending on the output power, but even within every line half cycle where the instantaneous input power changes permanently. A new continuous phase shedding strategy is presented which keeps the varying input power changes permanently. A new continuous phase shedding strategy is presented which keeps the varying input power changes permanently. A new continuous phase shedding strategy is presented which keeps the varying input power changes permanently. A new continuous phase shedding strategy is presented which keeps the varying input power changes permanently. A new continuous phase shedding strategy is presented which keeps the varying input power changes permanently. A new continuous phase shedding strategy is presented which keeps the varying input power changes permanently.

Due to the fact that the inductor current returns to zero in the off-time, a deviation in the inductance value would only cause a deviation in the inductor average current value and such an error would be compensated by the voltage controller.

However, an error in the voltage measurement could cause a drop out of the BCM. For such a case, entering into CCM has to be avoided to prevent overcurrent. Therefore it is beneficial to move slightly into DCM. A small extension of the switching period could also be beneficial for ZVS or near ZVS, if the switch-on instant is delayed until the occurrence of the first valley of the oscillating drain-source voltage. This is also done in most analog BCM implementations to reduce switching losses.

For changing into DCM, a factor $K_{lag} \geq 1$ is introduced (cf. Fig. 3). The period value for BCM is multiplied by the square of $K_{lag}$ to get the enlarged DCM switching period.
In order to retain the same average current also during DCM, the on-time also needs to be modified. It results as

\[ T'_s = T_s K_{lag}^2. \]  \hspace{1cm} (6)

By substituting (2), (5) and (6) in (7), the equation for the required on-time simplifies to

\[ T'_on = T_{on} K_{lag}. \]  \hspace{1cm} (8)

Using the enlarged on-time, the enlarged switching period can be calculated as

\[ T'_s = T'_on \frac{v_{out}}{v_{out} - v_{in}} K_{lag}. \]  \hspace{1cm} (9)

Hence (8) and (9) represent the control algorithm for DCM. Computation of any square root operation is not required.

The inductor current waveform at DCM is shown in Fig. 3.

**B. Closed-Loop Control Strategy**

The on-time feedforward calculation is performed without considering any parasitic effects of a real converter. In order to achieve an optimal power factor under all conditions an additional current controller can be applied. While with open-loop current control no current measurement is needed (cf. Fig. 1), the closed-loop control requires measurement of the input current, which can be realized with a single common shunt sensor. In Fig. 4 the control structure with closed current loop is shown. The on-time now is generated by adding the controller output value \( T'_{on} \) to the feedforward value \( T'_{on}^{ff} \) computed with (2):

\[ T_{on} = T'_{on} + T'_{on}^{ff}. \]  \hspace{1cm} (10)

The control-to-inductor-current transfer function can be directly derived from (1):

\[ G_i(s) = \frac{i_{avg}}{T_{on}} = \frac{v_{in}}{2L}. \]  \hspace{1cm} (11)

This transfer function exhibits pure proportional behavior. Due to the variable switching frequency a variation in the resulting dead-time has to be considered in a digital control structure.

Shifting into DCM by applying the factor \( K_{lag} \) the control-to-inductor-current transfer function becomes

\[ G'_i(s) = \frac{i_{avg}}{T_{on}} = \frac{v_{in}}{2LK_{lag}}. \]  \hspace{1cm} (12)

This indicates also a simple proportional behavior in DCM. \( K_{lag} \) only generates a larger dead-time in the digital control loop. The variation of the loop gain due to \( K_{lag} \) and the sinusoidally varying input voltage can be compensated by an adaptive controller gain.

**C. Current Balancing**

Due to tolerances in mass production the inductance value of each sample differs. This results in different inductor current slopes and consequently in a phase current mismatch in paralleled branches. Applying the same on-time for all inductors would result also in equal off-times and therefore collective BCM operation (cf. Fig. 5 a), or equal
DCM ratios, respectively. In this case the current difference corresponds with the inductance mismatch.

In some applications or operating points it can be necessary to ensure identical phase average or phase peak currents. In such a case current balancing is required.

Since all phases have to be operated with equal switching periods $T_s$ for an optimal (i.e. beat frequency-free) interleaving, every inductance needs an individual on-time to obtain equal average or peak currents.

The phase with the largest inductance $L_1$ becomes master phase to be operated in BCM which determines the master on-time and the global $T_s$. For equal average currents (cf. Fig. 5 b)) the on-time for the slave phase with inductance $L_2$ is calculated by multiplying the master on-time with the square-root of the inductance ratio [2]:

$$T_{on2} = T_{on1} \sqrt{\frac{L_2}{L_1}}$$  \hspace{1cm} (13)

For equal peak currents (cf. Fig. 5 c)) the master on-time is multiplied by the inductance ratio:

$$T_{on2} = T_{on1} \frac{L_2}{L_1}$$  \hspace{1cm} (14)

The determination of the inductor values and the calculation of the correction factors is required only once and can be done during an initial calibration sequence before the regular operation starts [2].

D. Phase Shedding and Frequency Limitation

One advantage of paralleling several phases is the potential to enhance the efficiency at light load conditions by adjusting the number of energized phases accordingly. Usually this feasibility is applied based on the load conditions. However, in a PFC application, there is a continuing variation in the input power within every mains half-cycle, for which reason phase shedding based on the instantaneous input power is promising. By changing the number of energized phases the average input current has to be allocated and results in a current reference step for every single phase. Since the inductor current in BCM and DCM is reset in every switching cycle, and a current reference step can be compensated within one switching cycle with the proposed control strategy, phase shedding can be performed at any time. Additionally, a phase current variation results in a change of the switching period. This property can be utilized to limit the switching frequency.

1) Conventional Phase Shedding

In general the levels of phase shedding are limited by the discrete number of interleaved phases. For example in a converter with $n = 3$ parallel phases there are 3 discrete interleaving modes (3 phases, 2 phases and single phase).

The adjustment of the input current is performed by tracking the on-time which is proportional to the inductor current:

$$T_{on,PS} = \frac{n}{k} \frac{2L}{v_{in}} \frac{i_{ref}}{n} = \frac{n}{k} T_{on}$$  \hspace{1cm} (15)

Where $k$ is the integer number of energized phases. For the switching period it follows

$$T_{s,PS} = \frac{n}{k} \frac{T_{on}}{v_{out}} \frac{v_{out}}{v_{in}} \frac{v_{out}}{v_{in}} = \frac{n}{k} T_s$$  \hspace{1cm} (16)

The effective switching frequency seen by the EMI filter can be represented as
\[ f_{s,\text{total}} = \frac{k^2}{n} \frac{1}{T_s}. \]  \hfill (17)

To retain optimal interleaving also the delay time of the phase shift needs to be adjusted. The phase shift delay is given by

\[ T_{\text{shift,PS}} = \frac{T_{\text{PS}}}{k}. \]  \hfill (18)

\[ f_{s,\text{total}} = \frac{n}{T_s K_{\text{tag}}^2} = \frac{k^2}{n} \frac{1}{T_s}. \]  \hfill (20)

where \( k \) represents the comparable number of active phases of the conventional phase shedding method. However, since \( K_{\text{tag}} \geq 1 \) is the range for DCM operation, \( k \) is no longer limited to integer values but rather can be a fractional value in the range \( n \geq k > 0 \). This enables a continuous change for the effective number of energized phases. The on-time and switching period are calculated using (8) and (9). The resulting effective switching frequency is identical to the result from conventional phase shedding (17).

The comparability of both phase shedding methods is illustrated in the measurement result of Fig. 6. The continuous phase shedding results in equal switching instants and input current shapes.

One drawback of continuous phase shedding are increased losses because optimal turn-off in the first valley of the oscillating drain-source voltage cannot be achieved in DCM, while with conventional phase shedding the converter is operated in BCM.

3) Switching Frequency Limitation

Due to the implementation of the control algorithms on a standard microcontroller, the maximum sampling and switching frequency is limited. Thus the frequency decreasing property of continuous phase shedding (cf. (20)) can be used to keep the switching frequency in a desired range. If the upper frequency limit is exceeded, \( k \) is decremented by a specified step size \( \Delta k \). When reaching the lower frequency threshold, \( k \) is increased, where the maximum value of \( k \) is \( n \). This process is illustrated in Fig. 7 for conventional discrete phase shedding (i.e. \( \Delta k = 1 \)) and for continuous phase shedding with \( \Delta k = 0.1 \). It can be seen that without or with discrete phase shedding a wide switching frequency range results. However, with continuous phase shedding, small switching frequency bands can be realized by choosing a proper \( \Delta k \).

In Fig. 7 c) it is illustrated that by reducing the number of energized phases the peak currents and accordingly the RMS currents increase and cause higher ohmic losses. However, this effect is more than compensated due to less switching events and thus reduced switching losses.

E. Current Limitation

Due to the fact that current sensing in every rail is not required for the proposed control strategy, information of the phase currents for overcurrent protection is not available.

Thus, the range of the on-time has to be limited to avoid overload. In BCM the maximum voltage controller output value \( V_{\text{ref,max}} \) is half of the maximum valid peak current \( i_{\text{pk,max}} \). With changing into DCM the increased on-time needs to be considered and the voltage controller output is limited to
\[ i_{ref,max} = \frac{i_{pk,max}}{2k_{tag}} \]  (21)

At closed-loop operation additionally the current controller output is limited to

\[ t_{on,max}^{adv} = \frac{i_{pk,max}L}{v_{in}} - t_{on}^{ff}. \]  (22)

Measured phase currents and the input current (i.e. current sum) were already shown above in Fig. 6 during phase shedding process with inactive current balancing, where all phases operate close to BCM (Fig. 6 a)) or in DCM (Fig. 6 b) at \( k = 2.0 \).

<table>
<thead>
<tr>
<th>TABLE I. PROTOTYPE INDUCTANCE VALUES</th>
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<tbody>
<tr>
<td>Inductance value</td>
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<tr>
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<tr>
<td>L1</td>
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<td>L2</td>
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For capturing the following measurement results the continuous phase shedding was enabled with the switching frequency range \( f_{s,toal} = 180 \text{ } \text{ } 390 \text{ } \text{ } kHz \).

The line voltage and current waveforms are shown in Fig. 8. Measured efficiency values for high and low line input voltage are depicted in Fig. 9. A power factor close to unity was achieved over a wide load range (cf. Fig. 10).

III. EXPERIMENTAL RESULTS

The described control concept depicted in Fig. 4 has been implemented on a microcontroller (TMS320F28035) for a prototype with \( n = 3 \) interleaved phases. The inductance values (cf. Table I) were intentionally designed with approx. 9% variation to simulate mass production tolerance.
It has been shown that current control of a PFC rectifier in boundary and discontinuous conduction modes can be established by a simple algorithm that is best suited to be realized as digital control even for high switching and sampling frequencies due to low computational effort. Current control can be realized without current measurement as feedforward control as well as closed-loop control. The DCM ratio can be controlled while still retaining the desired current average value.

The controller is also able to cope with interleaved operation of paralleled converters and to provide current balancing even in the case of inductance variations due to manufacturing tolerances.

The possibility of specific control of the DCM ratio leads to a novel scheme of fractional phase shedding in contrast to conventional phase shedding where only an integer number of phases can be turned off. This novel continuous degree of freedom can be used to minimize switching losses at light load and even during within a line half cycle or to keep the switching frequency within a narrow band.

REFERENCES


